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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/788,943	CHATTERJEE ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,18-25 and 27-40* is/are pending in the application.

4a) Of the above claim(s) *32-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,18-25,27-31 and 38-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a FINAL Office Action.

The amendment filed 5/16/2007 has been entered in view of the canceling claims 1-15, in response to the Notice Requiring Excess Claim Fees.

Claims 16-31 were previously examined.

Claims 32-37 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention.

Claims 1-15, 17, 26 have been cancelled.

Claims 38-40 are new.

Claims 16, 18-25, 27-31, 38-40 are under examination.

Claims 16, 18-25, 27-40 are still pending in the Application.

Objection to Claims 22-24 has been withdrawn in view of the amendment to claim 22.

Response to Amendment

Regarding cancelled claims 1-15, 17, 26, in accordance with (MPEP 714 R5 II), a claim being canceled must be indicated as "canceled;" the text of the claim must not be presented. Providing an instruction to cancel is optional. Canceled and not entered claims must be listed by only the claim number and status identifier, without presenting the text of the claims. When applicant submits the text of canceled or not-entered claims in the amendment, the Office may accept such an amendment, if the amendment otherwise complies with 37 CFR 1.121, instead of sending out a notice of non-compliant amendment to reduce the processing time. However, in this case, Applicant should

remove the text of the cancelled claims in the next communication, in response to the present Office Action.

Response to Arguments

Applicant's arguments filed 4/27/2007 have been fully considered but they are not persuasive.

In response to Applicant's arguments, regarding independent Claims 16 and 25, the Examiner concedes that Koschella fails to disclose "a non-volatile memory". However, under a new ground of rejection, in analogous art, Desmicht et al. (US 20060156033) discloses, Fig. 2, a chip CHP that includes a non-volatile memory NVM, including protection data ADA and protected data PDA, the protection data being intended to be used for authorizing/denying access to the protected data PDA by the microprocessor MP under the execution of a program PRO. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a non-volatile memory NVM as taught by Desmicht, in Koschella's processor-memory system, since non-volatile memories are more secure in storing protected data.

Applicant argues that Koschella uses a memory protection control register (MPCR) to authorize access to individual memory areas having a predetermined size in a memory device, while Applicant's claim 16 requires logic configured to authorize software to run on a CPU based on written information in a protected area of a non-volatile memory.

In response to Applicant's arguments, the memory protection control register (MPCR) 7 of Koschella merely holds the individual access authorizations associated with individual memory areas (B0, B1, . Bi, . Bn, Fig. 1). However, Koschella discloses logic device 5.1, Figs. 4-6, which is configured to authorize the CPU to access the memory device 3 by producing an area read enable signal REmemory i or an area write enable signal WE.memory i, respectively. Only if these signals correspond with the selected memory area Bi can this area be read from or written to. This is ensured by selecting only a single area Bi with the area read or write enable signal. The other areas are not selected. The area read or write enable signal will be produced only if the access authorization check in the logic device 5.1 using the signals RE, WE, OPC, CE.sub.memory i and the signals TEST and JTAG (not shown) determines an authorized access. In the event of an unauthorized access, the output of the signal RE.memory i or WE.memory i by the logic device 5.1 will be blocked.

Clearly, the authorization access is determined by the logic device 5.1, which authorizes the CPU to access selected memory areas in the memory device 3 by producing an area read enable signal RE.memory i or an area write enable signal WE.memory i, respectively, based on the signals RE, WE, OPC from the CPU and the signals TEST and JTAG (not shown).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16, 18-21, 25, 27, 28 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koschella (US-Patent No. 7,054,121) in view of Desmicht et al. (US 20060156033).

Regarding independent Claims 16, 25, Koschella discloses a processor-memory system with a protection circuit, Fig. 1, comprising:

A memory (memory device 3) including a protected area (B0, B1,Bi,. . Bn) or segments, that have to be treated differently in the event of an unauthorized external memory access, which is protected by a protection circuit 1.

A JTAG interface (externally accessible Data interface 6) known as Joint Test Action Group (JTAG), which is activated via a suitable external signal s1, which in the case of processors and microcontrollers is commonly referred to as "TEST" and "JTAG", respectively. Data d1 can be read or written into the memory device 3 through the externally accessible data interface 6.

Authorization logic (logic device 5.1, where the authorization logic device 5.1 is part of a controller (control circuit 5), which produces an area read enable signal $RE_{memory\ i}$ or an area write enable signal $WE_{memory\ i}$, respectively, for reading or writing in the selected memory area Bi, if the access authorization check in the logic device 5.1 using the signals RE, WE, OPC, $CE_{memory\ i}$ and the signals TEST and JTAG determines

an authorized access. The basic access permission for the selected memory area Bi is retrieved from the MPCR 7. In the event of an unauthorized access, the output of the signal $RE_{memory\ i}$ or $WE_{memory\ i}$, will be blocked by the logic device 5.1, as shown in Fig. 4, which is similar to that of Fig. 1.

Koschella discloses a processor-memory system with a protection circuit, Fig. 1, having memory device 3, which is integrated wholly or in part with the microcontroller, or forms a separate physical unit depending on the type of microcontroller and the amount of memory required. Koschella fails to disclose that the memory device in a non-volatile memory. However, the memory device may be implemented as a non-volatile memory, since there is nothing distinctly unique feature in a non-volatile memory that precludes the protection circuit disclosed by Koschella to operate properly with a microcontroller and a non-volatile memory.

In analogous art, Desmicht et al. (US 20060156033) discloses, Fig. 2, a chip CHP that includes a non-volatile memory NVM, including protection data ADA and protected data PDA, the protection data being intended to be used for authorizing/denying access to the protected data PDA by the microprocessor MP under the execution of a program PRO. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a non-volatile memory NVM as taught by Desmicht, in Koschella's processor-memory system, since non-volatile memories are more secure in maintaining the integrity of protected data, especially during power interruptions.

Regarding Claim 18, 27, Koschella discloses a processor CPU 2, Fig. 1, where the authorization logic device 5.1 combines the area signal $CE_{memory\ i}$ with the signal RE or WE from the CPU 2 to produce an area read enable signal $RE_{memory\ i}$ or an area write enable signal $WE_{memory\ i}$, respectively, for reading or writing in the selected memory area Bi. 9

Regarding Claims 19-21, 28, Koschella discloses CPU2 initiating associated control instructions (e.g., reading or writing) for the memory device 3 during the regular operating cycle, for reading or writing data in an unprotected area of the memory device 3, where the unprotected area does nor require authorization access the authorization logic device 5.1. The JTAG interface (externally accessible Data interface 6) known as Joint Test Action Group (JTAG) is activated via a suitable external signal s1, which in the case of processors and microcontrollers is commonly referred to as "TEST" and "JTAG", respectively. Data d1 can be read or written into the memory device 3 through the externally accessible data interface JTAG 6, or data (D0, .Dn,) can be read or written from the CPU2 during different times.

Regarding Claims 38-40, Koschella discloses via a reset input R, the flip-flop 11 can be set to the "0" state by an internally or externally generated set-reset signal S/R. This is appropriate upon power-up, because in this unstable operating state no memory access should take place. The inhibit action "1" is also forced via the set-reset signal S/R at a set input S of the flip-flop 12 independently of other signals (for instance at start-up), Fig. 6.

Claims 22-24 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koschella (US-Patent No. 7,054,121) in view of Desmicht et al. (US 20060156033) and further in view of Golshan (US Patent No. 6,671,841).

Regarding Claims 22- 24, 29-31, Koschella substantially discloses a read enable signal RE or write enable signal WE generated from the CPU 2 and derived from a system CPU clock (not shown), for "reading" or "writing" data in memory device 3, Fig. 8. A JTAG clock is externally provided to the externally accessible data interface JTAG 6, where the two clocks are asynchronous with respect to each other. For a person skilled in the art, it is well known that the JTAG external clock is slower that the system CPU clock. Nevertheless, Koschella in combination with Desmicht does not explicitly disclose a synchronization buffer for synchronizing signals between JTAG, CPU interface and the controller.

In analogous art, Golshan (US Patent No. 6,671,841) discloses a "synchronizer 140" for synchronizing a JTAG clock "TCK 125" to a system clock CPU clock "CLK 135", as shown in the block diagram of a system 10, Fig. 1B and in the flow diagram of a method 400, Fig. 4). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a synchronizer as taught by Golshan, in the combined device of Koschella and Desmicht, for eliminating clock skewing associated with asynchronous clocks.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on 571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Primary Examiner
Art Unit 2117

6/11/07

JAMES C. KERVEROS
PRIMARY EXAMINER

Date: 11 June 2007
Office Action: Final Rejection

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